SEMESTER S6

SYSTEM ON CHIP DESIGN

Course Code	PCEVT602	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs.30 Min.
Prerequisites (if any)	PCEVT501 Digital CMOS Design	Course Type	Theory

Course Objectives:

1. Understand the SoC design process, including the differences between waterfall and spiral models, and the significance of top-down versus bottom-up approaches in meeting specification requirements.
2. Develop the ability to create a comprehensive design specification and execute top-level macro design, utilizing appropriate tools and methodologies for macro integration and productization.
3. Apply best practices in RTL coding, with a focus on proper clock and reset handling to ensure reliable and efficient design implementation.
4. Master the design and integration of hard macros, addressing key issues such as design for testability, power distribution, and model development, to produce robust and deliverable macro products.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	System On Chip Design Process: A canonical SoC Design, SoC Design flow - Waterfall vs spiral, Top-down vs Bottom up, Specification requirement, Types of specification, System design process, System level design issues- Soft IP vs Hard IP.	9
2	Macro Design Process: Contents of a design specification, Top level Macro Design,Top level Macro Design Process, Activities and tools, Subblock design, Macro integration, Soft macro productization.	9
3	RTL coding guidelines: Overview of coding guidelines, Guidelines for	9

	clocks and resets - Mixed clock edges, Clock buffers, Gated clocks, Internally generated clocks, Gated clocks, Internally generated resets.	
4	Developing hard macros: Design issues for hard macros – Design for test, Clock and reset, Aspect ratio, Porosity, Pin placement, Power distribution. The hard macro design process, Block integration for hard macros, Productization for hard macros, Model development for hard macros, Soft macro deliverables, Hard macro deliverables.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the SoC design flow, differentiate between design methodologies, and address system-level design issues.	**K2**
CO2	Develop and implement design specifications for macro design, including integration and productization of soft macros.	**K3**
CO3	Demonstrate proficiency in applying RTL coding guidelines, effectively managing clocks and resets in their designs.	**K3**
CO4	Design, integrate, and productize hard macros, with an understanding of design issues and deliverables specific to hard macro development	**K4**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**1**	**1**	**1**				**1**			
CO2	**3**	**3**	**2**	**1**	**1**				**1**			
CO3	**3**	**3**	**2**	**1**	**2**				**1**			
CO4	**3**	**3**	**2**	**2**	**2**				**1**	**1**		**1**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Reuse Methodology manual for System-On-A-Chip Designs	Michael Keating, Pierre Bricaud	Springer	2002
2	System-on-Chip Design with Arm® Cortex® -M Processors	JOSEPH YIU	arm Education Media	2019
3	Digital VLSI Chip Design with Cadence and Synopsys CAD Tools	Erik Brunvand	Pearson	1st, July 2009
4	SoC Verification-Methodology and Techniques,	Prakash Rashinkar, Peter Paterson and Leena Singh,	Kluwer Academic Publishers,	2001

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital systems Testing and testable Design	Miron Abramovici, Melvin A. Breur, Arthur D. Friedman	Jaico Publishing House,	2001
2	Hardware Design Verification: Simulation and Formal Method-based Approaches	William K.Lam	Prentice Hall Professional Technical Reference	2005
3	Design of System on a ChipDevices & Components	Ricardo Reis, Jochen A. G. Jess	Springer	2004

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/108106191
2	https://nptel.ac.in/courses/108106177
3	https://nptel.ac.in/courses/106105161
4	https://www.arm.com/why-arm/custom-socs
5	https://www.youtube.com/watch?v=dokgLSAhqHI