SEMESTER S5

CAD BASED VLSI DESIGN OPTIMIZATION

Course Code	PEEVT525	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	5/3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	5 Credit Elective

Course Objectives:

1. Understand the different stages of design flow; the basic data structures and algorithms used in each stage
2. Understand data structures and algorithms used in recent CAD tools
3. Identify suitable data structures and propose new algorithms for CAD applications and develop new CAD tools

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Graph Terminology: Basic graph theory terminology, Data structures for representation of Graphs Search Algorithms: Breadth First Search, Depth First Search, Topological Sort Shortest Path Algorithms: Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path	9
2	The VLSI Design Problem, The Design Domains, A Quick Tour of VLSI Design Automation Tools: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods VLSI Design Flow, VLSI Design Styles Partitioning: Levels of Partitioning, Parameters for Partitioning, Classification of Partitioning Algorithms, Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm	9
3	**Layout**: Layout Layers and Design Rules, Physical Design Optimizations	9

	Compaction: Applications of Compaction, Informal Problem Formulation, Graph Theoretical Formulation, Maximum Distance Constraints, Longest Path algorithm for DAG, Liao-Wong Algorithm, The Bellman-Ford Algorithm **Placement**: Optimization Objectives, Wirelength Estimation, Weighted Wirelength, Maximum Cut Size, Wire Density Placement Algorithms: Constructive Placement, Iterative Improvement Partitioning: The Kernighan-Lin Partitioning Algorithm	
4	**Floorplanning**: Optimization Objectives, Slicing Floorplan, Non-Slicing Floorplan. Floorplan Representations: Constraint Graph, Sequence Pair **Global Routing**: Terminology and Definitions, Optimization Goals, Representation of Routing Regions Maze Routing Algorithms: Lee's Algorithm, Detailed Routing: Horizontal and Vertical Constraint Graph. Channel Routing Algorithms: Left-Edge algorithm General Remarks on VLSI Simulation.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Internal Ex	Evaluate	Analyse	Total
5	**15**	**10**	**10**	**40**

Criteria for Evaluation (Evaluate and Analyse): 20 marks

1. Literature Review and Report (10 Marks)

Assessment Method:

- Students review recent publications on a specific topic related to VLSI design (e.g., advancements in layout optimization or new algorithms for partitioning).
- Preparation of a detailed report summarizing the findings, discussing the significance, and suggesting potential improvements or future research directions.

Criteria:

- Relevance of Chosen Publications (2 Marks): Selection of up-to-date and relevant research papers.

- Depth of Analysis (4 Marks): Thorough understanding and critical analysis of the literature.
- Clarity and Organization (2 Marks): Well-structured and clearly written report.
- Originality (2 Marks): Innovative insights or perspectives on the topic.

2. VLSI Design Flow Understanding and Report (5 Marks)

Assessment Method:

- Students study the VLSI design flow, including partitioning, placement, and floor planning.
- Preparation of a comprehensive report explaining each step of the design flow, the tools used, and their features.

Criteria:

- Comprehensiveness (2 Marks): Detailed explanation of each step in the VLSI design flow.
- Tool Proficiency (1 Mark): Understanding of the various EDA tools used in the design process.
- Clarity and Detail (1 Mark): Clear and detailed presentation of information.
- Analytical Skills (1 Mark): Critical analysis of the design flow and tool features.

3. Graph Theory and Algorithms Practical Assignment (5 Marks)

Assessment Method:

- Students implement and test various graph algorithms (e.g., Dijkstra's algorithm, Floyd-Warshall algorithm) using appropriate data structures.
- Submit a report with their implementation, test cases, and performance analysis.

Criteria:

- Correctness of Implementation (2 Marks): Accurate implementation of graph algorithms.
- Performance Analysis (1 Mark): Detailed analysis of the algorithm performance on different test cases.
- Clarity and Presentation (1 Mark): Well-organized and clearly written report.
- Problem-Solving Skills (1 Mark): Ability to troubleshoot and optimize the implementation.

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. Each question carries 9 marks. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply Search Algorithms and Shortest Path Algorithms to find various graph solutions.	**K3**
CO2	Apply partitioning algorithms on graphs representing netlist.	**K3**
CO3	Apply different algorithms for layout compaction and placement	**K3**
CO4	Utilise different algorithms to solve floorplan and routing problems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2							1		
CO2	3	3	2							1		
CO3	3	3	2							1		
CO4	3	3	2							1		

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	"Algorithms for VLSI Design Automation",	Gerez,Sabih H.	John Wiley & Sons	2006.
2	Algorithms for VLSI Physical Design Automation	Sherwani, Naveed A	Kluwer Academic Publishers	1999
3	VLSI Physical Design: From Graph Partitioning to Timing Closure	Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng	Springer	2011

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Physical Design Automation: Theory and Practice	Sadiq M. Sait and H. Yousse	World Scientific	1999
2	Introduction to Algorithms.	Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest	The MIT Press	3rd edition, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/hk5rQs7TQ7E?feature=shared
2	https://youtu.be/O9guSe5_tG0
3	https://youtu.be/F44WOxhbtV0
4	https://youtu.be/TYy2o8Qy4TY

SEMESTER: S5

DIGITAL IC DESIGN LAB

Course Code	PCEVL507	CIE Marks	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	ESE Marks	50
Credits	2	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304 Logic Circuit Design PCEVT402 Digital System Design	Course Type	Lab

Course Objectives:

1. Develop a fundamental understanding of digital logic gates and their implementation using Verilog.
2. Learn the principles of designing and implementing basic combinational and sequential circuits.
3. Develop the ability to synthesize complex digital circuits using EDA tools such as FOSS tools, Cadence, and Synopsys.
4. Gain experience in using synthesis tools to optimize and implement digital circuits

Details of Experiment

Expt. No	Experiment
1	Write Verilog codes to realize the logic gates: AND, OR, NOT, XOR and XNOR
2	Write Verilog codes to realize a 2-bit half adder in all three modeling styles
3	Write a structural Verilog code to realize a 2-bit full adder
4	Write a Verilog code to realize a 2-bit full adder using two half adders
5	Write a behavioural Verilog code to realize a 8:1 MUX
6	Write a behavioural Verilog code to realize a 1:16 DE-MUX
7	Write a behavioural Verilog code to realize a 16:4 encoder
8	Write a behavioural Verilog code to realize a 3:8 decoder
9	Write Verilog codes to realize SR, D, JK and T flip-flops
10	Realize a 3-bit comparator in Verilog using behavioural and structural modeling

11	Realize ring and Johnson counters in Verilog using data-flow modeling
12	Realize a BCD counter in Verilog using gate level abstraction (structural modeling)
13	Synthesize the basic logic gates using FOSS/Cadence/Synopsys tool
14	Synthesize both half adder and full adder using FOSS/Cadence/Synopsys tool
15	Realize a FIFO in Verilog and synthesize using FOSS/Cadence/Synopsys tool

Course Assessment Method (CIE: 50 Marks, ESE 50 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work, experiments, Viva and Timely completion of Lab Reports / Record. (Continuous Assessment)	Internal Exam	Total
5	25	20	50

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

Mandatory requirements for ESE:

- Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.
- Endorsement by External Examiner: The external examiner shall endorse the record.

Course Outcomes (COs)

At the end of the course the student will be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Demonstrate the ability to write Verilog code to implement fundamental logic gates and verify the functionality of implemented logic gates through simulation and testbenches.	**K2**
CO2	Get familiarity in various modeling styles (behavioral, dataflow, and structural) to realize combinational and sequential circuits.	**K2**
CO3	Demonstrate the ability to synthesize Verilog code for complex digital circuits using EDA tools such as FOSS, Cadence, and Synopsys.	**K3**
CO4	Ability to use synthesis tools to optimize digital circuits for performance, area, and power.	**K4**
CO5	Ability to produce and present detailed reports on the synthesis and optimization process	**K5**

K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3			2							
CO2	2	3			2							
CO3	3	3	3		3							
CO4	2	3	3	3	3							

1: Slight (Low),2: Moderate (Medium),3: Substantial (High), : No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL Synthesis: A Practical Primer	J. Bhasker	B. S. Publications,	2001
2	Fundamentals of Logic Design	Roth C.H	Jaico Publishers. V Ed., 2009	5th Edition
3	Digital Principles & Design	Donald G Givone	McGraw Hill Education	2017
4	Digital Design: Principles and Practices	John F Wakerly	Pearson India	4th, 2008

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL : A guide to digital design and synthesis	Palnitkar S.,	Prentice Hall; 2003.	2nd Edn.,
2	ASIC Design and Synthesis RTL Design Using Verilog	Vaibbhav Taraate	Springer	2021
3	FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version	Pong P. Chu	Wiley	2008

Video Links (NPTEL, SWAYAM…)	
Sl. No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/
2	https://archive.nptel.ac.in/courses/117/106/117106086/

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. Lab Reports and Record Keeping (6 Marks)

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. Viva Voce (5 Marks)

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. Procedure/Preliminary Work/Design/Algorithm (10 Marks)

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.

- Creativity and logic in algorithm or experimental design.

2. Conduct of Experiment/Execution of Work/Programming (15 Marks)

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. Result with Valid Inference/Quality of Output (10 Marks)

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. Viva Voce (10 Marks)

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. Record (5 Marks)

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER S5

FPGA LABORATORY

Course Code	**PCEVL508**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304 Logic Circuit Design PCEVT402 Digital System Design	**Course Type**	Lab

Course Objectives:

1. Equip students with the skills to write, test, and debug VHDL code for various digital circuits.
2. Enable students to design and implement basic digital components such as logic gates, multiplexers, adders, counters, and registers on FPGA.
3. Enable students to design and implement sequential circuits, including various types of flip-flops, sequence detectors, and counters, on FPGA.
4. Guide students in designing, implementing, and optimizing complex digital systems, such as ALUs and FIFO buffers, on FPGA.

Details of Experiment

Expt. No	Experiment
1	Realize basic the logic gates in VHDL and implement on FPGA
2	Realize a 4:1 MUX in VHDL and implement on FPGA
3	Realize a 1:8 DEMUX in VHDL and implement on FPGA
4	Realize a half adder in VHDL and implement on FPGA
5	Realize a full adder in VHDL and implement on FPGA
6	Realize a 2-bit comparator in VHDL and implement on FPGA
7	Realize a 4-bit shift register in VHDL and implement on FPGA
8	Realize a FIFO in VHDL and implement on FPGA
9	Realize a 4-bit adder in VHDL and implement on FPGA
10	Realize a Up/Down counter in VHDL and implement on FPGA
11	Realize a Mealy and Moore sequence detector to detect the sequence 1010 in VHDL and

	implement on FPGA
12	Realize an asynchronous BCD counter in VHDL and implement on FPGA
13	Realize a 4-bit Gray to Binary in VHDL and implement on FPGA
14	Realize the flipflops D, JK and T in VHDL and implement on FPGA
15	Realize in VHDL a 4-bit ALU that performs basic arithmetic (addition, subtraction) and logic (and, or, xor) operations on 4-bit inputs and implement on FPGA . Understand the synthesis reports and perform timing and power analysis.

Course Assessment Method (CIE: 50 Marks, ESE 50 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work, experiments, Viva and Timely completion of Lab Reports / Record. (Continuous Assessment)	Internal Exam	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	**15**	**10**	**10**	**5**	**50**

Mandatory requirements for ESE:

- Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.
- Endorsement by External Examiner: The external examiner shall endorse the record.

Course Outcomes (COs)

At the end of the course the student will be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Write, test, and debug VHDL code to accurately describe and implement a variety of digital circuits.	**K2**
CO2	Design and implement fundamental digital components, such as logic gates, multiplexers, adders, and counters, using FPGA technology.	**K3**
CO3	Design, implement, and analyze sequential circuits, including flip-flops, sequence detectors, and various types of counters, on FPGA.	**K3**
CO4	Integrate multiple digital components into complex systems, such as ALUs and FIFO buffers, and optimize these systems for performance and resource efficiency on FPGA.	**K4**

K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3			2				1			
CO2	2	3			2				1			
CO3	3	3	3		3				1			
CO4	2	3	3	3	3				2			

1: Slight (Low),2: Moderate (Medium),3: Substantial (High), : No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Design with RTL Design, VHDL, and Verilog	Frank Vahid	Wiley	2010
2	VHDL for Engineers	Kenneth L. Short	Pearson	1st Edition, 2008
3	FPGA Prototyping by VHDL Examples: Xilinx MicroBlaze MCS SoC	Pong P. Chu	Wiley	2018
4	Digital Systems Design Using VHDL	Charles H. Roth Jr., Lizy Kurian John	Cengage Learning	2007

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VHDL: Programming by Example	Douglas L. Perry	McGraw-Hill	4th Edition, 2002
2	Circuit Design with VHDL	Volnei A. Pedroni	MIT Press	2nd Edition, 2010
3	The Designer's Guide to VHDL	Peter J. Ashenden	Morgan Kaufmann	3rd Edition, 2008

Video Links (NPTEL, SWAYAM…)	
Sl. No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/108/117108040/
2	https://nptel.ac.in/courses/108106177

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. Lab Reports and Record Keeping (6 Marks)

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. Viva Voce (5 Marks)

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. Procedure/Preliminary Work/Design/Algorithm (10 Marks)

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.

- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
- Creativity and logic in algorithm or experimental design.

2. Conduct of Experiment/Execution of Work/Programming (15 Marks)

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. Result with Valid Inference/Quality of Output (10 Marks)

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. Viva Voce (10 Marks)

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. Record (5 Marks)

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER 6

Electronics Engineering (VLSI Design and Technology)

SEMESTER 6

ANALOG VLSI DESIGN

Course Code	PCEVT601	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-1-0-0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs.30 Min.
Prerequisites (if any)	PCECT302,PCECT303	Course Type	Theory

Course Objectives:

1. A foundation in the fundamentals of Analog VLSI Design
2. Ability to Design of IC MOS Amplifiers and PLL
3. An Introduction to challenges facing in Analog IC Design

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**2-Terminal MOS Structure** - Flat Band Voltage, Potential Balance and Charge, Effect of Gate-Body Voltage on Surface Condition General Analysis. Inversion: Strong and Weak Inversion, Small Signal Capacitance.	11
2	**3-Terminal MOS Structure** - Contacting Inversion Layer, General Analysis, Body-effect, Pinch-off voltage. Introduction, Regions of Operation.	11
3	**4-Terminal MOS Structure** – Introduction, Complete All-Region Model – Current Equations, Simplified All-Region Models: Linearizing Depletion Region Charge, Source-Referenced Simplified All- Region Models. Strong Inversion: Complete Strong Inversion Model- Non Saturation	11
4	**Single-Stage Amplifiers** - Introduction to basic amplifier Configurations: Gate-Drain Connected Loads: CS, Frequency Response, Noise Analysis, Current-Source Load: CS (only CS) Cascode, Push-pull amplifier **Noise**:Types of Noise: Thermal, Flicker, Shot Noise.	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Gives students structural idea about 2 terminal MOSFET.	**K2**
CO2	Gives students structural idea about 3 terminal MOSFET	**K2**
CO3	This module gives students structural idea about 4 terminal MOSFET and strong inversion models.	**K1**
CO4	This module deals about Single stage amplifiers and its active loads and different types of Noises.	**K1**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	1									
CO2	3	3	-									
CO3	2	2	-									
CO4	3	2	1									

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Operation and Modeling of the MOS Transistor	YannisTsividis Colin McAndrew	3/e, 2010	OUP
2	CMOS – Circuit Design, Layout, andSimulation	R. Jacob Baker, Harry W Li,David E Boyce	1998.	3rd Edition, .
3	Design of Analog CMOS Integrated Circuits	BehzadRazavi	2008	Tata McGraw Hill
4	CMOS Analog Circuit Design	Philip E Allen, Douglas R Holberg	2010	International Student(Second) Edition, First Indian Edition
5	CMOS – Circuit Design, Layout, andSimulation	R. Jacob Baker, Harry W Li,David E Boyce	1998.	3rd Edition, .

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS, CIRCUIT Design, Layout and Simulation	Baker, Harry, David	3/e	PHI

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/117101105
2	https://nptel.ac.in/courses/117101105
3	https://nptel.ac.in/courses/117101105
4	https://nptel.ac.in/courses/117101105