SEMESTER S5

CAD FOR VLSI DESIGN

Course Code	PEEVT524	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. Understand the different stages of design flow; the basic data structures and algorithms used in each stage
2. Understand data structures and algorithms used in recent CAD tools
3. Identify suitable data structures and propose new algorithms for CAD applications and develop new CAD tools

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Graph Terminology: Basic graph theory terminology, Data structures for representation of Graphs Search Algorithms: Breadth First Search, Depth First Search, Topological Sort Shortest Path Algorithms: Dijkstra's Shortest-Path Algorithm for single pair shortest path, Floyd Warshall Algorithm for all pair shortest path	9
2	VLSI Design Flow, VLSI Design Styles Partitioning: Levels of Partitioning, Parameters for Partitioning, Classification of Partitioning Algorithms, Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm	9
3	**Layout**: Layout Layers and Design Rules, Physical Design Optimizations Compaction: Applications of Compaction, Informal Problem Formulation, Graph Theoretical Formulation, Maximum Distance Constraints, Longest Path algorithm for DAG, Liao-Wong Algorithm. **Placement**: Optimization Objectives, Wirelength Estimation, Weighted	9

	Wirelength, Maximum Cut Size, Wire Density Placement Algorithms: Quadratic Placement	
4	**Floorplanning**: Optimization Objectives, Slicing Floorplan, Non-Slicing Floorplan. Floorplan Representations: Constraint Graph, Sequence Pair **Global Routing**: Terminology and Definitions, Optimization Goals, Representation of Routing Regions Maze Routing Algorithms: Lee's Algorithm, Detailed Routing: Horizontal and Vertical Constraint Graph. Channel Routing Algorithms: Left-Edge algorithm	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply Search Algorithms and Shortest Path Algorithms to find various graph solutions.	**K3**
CO2	Apply partitioning algorithms on graphs representing netlist.	**K3**
CO3	Apply different algorithms for layout compaction and placement	**K3**
CO4	Utilise different algorithms to solve floorplan and routing problems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	2							1		
CO2	3	3	2							1		
CO3	3	3	2							1		
CO4	3	3	2							1		
CO5												

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	"Algorithms for VLSI Design Automation",	Gerez,Sabih H.	John Wiley & Sons	2006.
2	Algorithms for VLSI Physical Design Automation	Sherwani, Naveed A	Kluwer Academic Publishers	1999
3	VLSI Physical Design: From Graph Partitioning to Timing Closure	Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng	Springer	2011

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Physical Design Automation: Theory and Practice	Sadiq M. Sait and H. Yousse	World Scientific	1999
2	Introduction to Algorithms.	Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest	The MIT Press	3rd edition, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/hk5rQs7TQ7E?feature=shared
2	https://youtu.be/O9guSe5_tG0
3	https://youtu.be/F44WOxhbtV0
4	https://youtu.be/TYy2o8Qy4TY