SEMESTER S5

VLSI TECHNOLOGY

Course Code	**PCEVT503**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCECT302	**Course Type**	Theory

Course Objectives:

1. To give knowledge about IC fabrication techniques and VLSI design methodologies.
2. To impart the skill of analysis and design of MOSFET and CMOS logic circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Material Preparation- Purification, Crystal growth (CZ process), wafer preparation. Thermal Oxidation- Dry and Wet oxidation, Diffusion- diffusion techniques. Ion implantation -Technique, annealing. Epitaxy: Vapour phase epitaxy and molecular beam epitaxy Lithography- Photo lithographic sequence, Electron Beam Lithography. Etching and metal deposition, CMOS Twin well process	9
2	Moore's law. ASIC design, Full custom ASICs, Standard cell based ASICs, Gate array based ASICs, SoCs, FPGA devices, ASIC and FPGA Design flows, Top-Down and Bottom-Up design methodologies. Logical and Physical design. Speed power and area considerations in VLSI design	9
3	CMOS inverters- DC characteristics, switching characteristics, power dissipation , Layout Design rules, Stick Diagram and layout of CMOS Inverter, two input NAND and NOR gates.	9

	MOSFET Logic Design -Pass transistor logic, Complementary pass transistor logic and transmission gate logic , realization of functions	
4	Read Only Memory-4x4 MOS ROM Cell arrays(OR,NOR,NAND) Random Access Memory –SRAM-Six transistor CMOS SRAM cell, DRAM –Three transistor and One transistor Dynamic Memory Cell	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Summarize MOSFET fabrication techniques	**K2**
CO2	Outline the various methodologies in ASIC and FPGA design.	**K2**
CO3	Understand CMOS technology.	**K2**
CO4	Design VLSI Logic circuits with various MOSFET logic families.	**K2**
CO5	Compare different types of memory elements	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**											**3**
CO2	**2**											**3**
CO3	**2**	**2**	**2**		**2**							**3**
CO4	**2**	**2**	**2**		**2**							**3**
CO5	**2**											**3**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Introduction to VLSI Circuits and Systems,	John P Uyemura,	Wiley India,	2006
2	VLSI Technology	S.M. SZE	McGraw-Hill	Indian Edition,2/e,,2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Integrated Circuits- A Design Perspective	Jan M. Rabaey	Prentice Hall	Second Edition, 2005
2	Principles of CMOS VLSI Design-A Systems Perspective	Neil H.E. Weste , Kamran Eshraghian	Pearson Publication	Second Edition,2005
3	Design of Analog CMOS Integrated Circuits	Razavi	McGraw Hill Education India Education, New Delhi	1e,2003.
4	CMOS Digital Integrated Circuits- Analysis & Design	Sung –Mo Kang & Yusuf Leblebici,	McGraw-Hill,	Third Ed., 2003.
5	Fundamentals of Modern VLSI Devices	Yuan Taur & Ning,	Cambridge University Press,	2008

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/Iv4Cj2A3ldw?si=8wkrFXV583vMiJDh, https://youtu.be/fokSc0xlTfM?si=pbWd_UtVbvVacPA,
2	https://youtu.be/oZSv68esbgI?si=AoGIe2JX9G6GsdYZ, https://youtu.be/4cPkr1VHu7Q?si=alAxpL5vUn9s24zX, https://youtu.be/ht7nEjNydDU?si=_E7m1qMrUvqdcya4
3	https://youtu.be/UuafwIJAKhY?si=PRrPHzB4mWxwm5h7
4	https://youtu.be/Y8FvvzcocT4?si=3anWLYD00aACws9y