SEMESTER S5

DIGITAL CMOS DESIGN

Course Code	**PCEVT501**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3-1-0-0	**ESE Marks**	60
Credits	4	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Theory

Course Objectives:

1. This Course aims to offer distinctive coverage of the dynamic and static circuits and to discuss important aspects of timing and synchronisation, power dissipation, interconnect packing, and signal integrity in real-world system design

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**MOS TRANSISTOR PRINCIPLES** Introduction to CMOS technology: CMOS logic, CMOS fabrication and layout, Design partitioning, Circuit design, Physical Design, Design verification, Fabrication, Packaging and testing. **MOS transistor**: MOS Transistor Basics, Secondary Effects, Process Variations, Technology Scaling.	11
2	**Static and Dynamic circuits:** **CMOS Inverter:** Static CMOS Inverter: DC Characteristics, Beta Ratio Effects, Noise margin. Other static CMOS logic gates, static properties (2 input NAND, NOR), Combinational logic circuits. **Fundamentals of dynamic logic**: Dynamic pass transistor circuits, High performance dynamic circuits-Domino CMOS, Multi Output Domino Logic, Dual-rail Domino Logic, NP Domino logic (NORA) logic.	11
3	**Designing arithmetic building blocks:** Adders: Design considerations, Fast adders, Multipliers, Barrel Shifters, Speed and Area Trade-offs. **Semiconductor Memories**: Memory Design, SRAM, DRAM structure and	11

	implementations	
4	**Interconnect effects**: Introduction, Wire Geometry, Interconnect Modelling: Resistance, Capacitance, and Inductance. Interconnect Impact: Delay, Energy, Crosstalk, Inductive Effects, Effective Resistance and Elmore Delay.	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
● 2 Questions from each module. ● Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	● Each question carries 9 marks. ● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand the basics of MOS Transistors and CMOS Inverter.	**K2**
CO2	Design Static and Dynamic Logic circuits.	**K3**
CO3	Design arithmetic and logic circuits and memory elements.	**K3**
CO4	Simulate and calculate the impacts of R, L, and C parasitic, the effects of technological scaling, ways to deal with capacitive crosstalk, calculate the RC delay, and inductive effects.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**										
CO2	**3**	**3**										
CO3	**3**	**3**	**2**									
CO4	**3**	**3**										

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Integrated Circuit Design	Neil H. E. Weste and David Money Harris	Pearson Education.	4/e, 2011
2	CMOS Digital Integrated Circuits	Sung-Mo Kang, Yusuf Leblebici	Tata McGraw-Hill Education	3/e, 2003
3	Digital Integrated Circuits – A Design Perspective	Rabaey, Chandrakasan and Nikolic	Pearson Education.	2/e

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS, Circuit Design, Layout, and Simulation	R. Jacob Baker, Harry W. Li, David E. Boyce	Wiley Interscience	3/e
2	Introduction to VLSI Circuits and Systems	John P. Uyemura	John Wiley & Sons, Inc.	

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc22_ee08/preview, https://nptel.ac.in/courses/117103066,
2	https://onlinecourses.nptel.ac.in/noc22_ee08/preview
3	https://www.youtube.com/watch?v=8LRMqA5ZPss, https://archive.nptel.ac.in/courses/117/101/117101058/
4	https://archive.nptel.ac.in/courses/117/103/117103066/